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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/926,454 | 11/06/2001 | Syouji Higashida | 107400-00044 | 4669 |

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| EXAMINER | |
|---|---|
| MONDT, JOHANNES P | |
| ART UNIT | PAPER NUMBER |
| 2826 | |

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/926,454 | HIGASHIDA ET AL. | |
| | Examiner | Art Unit | |
| | Johannes P Mondt | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2-6,8 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6,8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/28/2003 has been entered.

### *Response to Amendment*

Amendment filed 11/28/2003 with aforementioned Request for Continued Examination has been entered and forms the basis of this office action. Applicant cancelled claims 1 and 7 and, not quite in accordance with the first sentence on page 2, Applicant amended claims 2, 3, 4, 5 and 6. Applicant added new claims 8 and 9. Comments on Remarks appended to said Amendment are included below under "Response to Arguments".

### *Priority*

2. Acknowledgment is made of applicant's claim for priority under 35 U.S.C. 119(a)-(d) based upon an application filed in Japan on 01/12/2000. A claim for priority cannot be based on said application, since the PCT application was filed more than one year later.

***Response to Arguments***

3. Applicant's arguments filed 11/28/2003 have been fully considered but they are not completely persuasive: although grounds for the rejection under 35 USC 112, first paragraph, have been convincingly countered by the amendment filed 11/28/2003, the art rejections on previous claims 1-6 and 7 as based on Williams et al and Yamamoto (and Throngnumchai for claim 7) can be readily amended to apply to the amended claim set. Furthermore, the Specification is objected to for inconsistencies as pointed out below. Also included are objections to the claim language for minor informalities.

***Claim Objections***

4. ***Claims 8 and 9*** are objected to because of the following informalities: the wording "to break down an input of a constant voltage or more applied between said gate and said source" (lines 5-6 in claim 8; lines 5-6 in claim 9) should be replaced by: "to prevent breakdown due to a voltage at or above a certain value". Appropriate correction is required.

5. ***Claim 9*** is objected to because of the following informalities: the wording "of said of said" (line 11) should be replaced by: "of said". Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claim 8 and 2-6*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al (6,268,242 B1) in view of Yamamoto (JP10144938A).

*On claim 8 (which is the independent claim):* Williams et al teach a semiconductor device (cf. title) comprising:

an insulating gate field effect transistor comprising a plurality of transistor cells (separated by a width W; see Figure 1) which are arranged in a semiconductor layer 108 (cf. column 3, lines 39-40) and connected in parallel; and

a protective diode D1 (and D2) (cf. column 3, lines 58-64) connected between a gate and a source of said insulating gate field effect transistor to break down an input of a constant voltage or more applied between said gate and said source (inherent in diode), wherein said protective diode is formed as a bi-directional diode in which one or more ring-shaped p-type layers and one or more ring-shaped n-type layers 130 (cf. column 3, lines 58-64) are flatly and alternately provided on an insulating layer 132 (cf. column 3, line 60) at a peripheral portion of a region of said transistor cells, a source wiring 112 (cf. column 3, line 62) (cf. Figures 7A and 7B) contacts with the innermost

layer of said protective diode, and a metal film 134, said metal film being ring-shaped (that the ring is open is a different matter, covered by the remainder of the claim language (final two lines of claim) and addressed below in connexion with the relevant claim language), contacts with the outermost layer of said protective diode (cf. col. 3, l. 58-63), said metal film 134 being successively formed with a gate electrode pad 710 comprising a metal film (cf. col. 3, l. 58-63, Figure 7B).

*Williams does not necessarily teach* the metal film 134 to be contacting the full circumferential length of the outermost layer. However, it would have been obvious to improve the invention by Williams to include such ring-shaped contacts in view of Yamamoto, who teaches for the specific purpose of increasing the electrostatic strength of a Zener diode that said Zener diode and its contact metal be formed so as to *encircle* the cell region (see Abstract, "Problem to be Solved", first sentence).

*Motivation* to include the teaching in this regard by Yamamoto is the consequent improvement of the capability of the Zener diode to protect against electrostatic discharge. The inventions can be *combined* in this regard, because the contact area between the inner – and outermost Zener diode p-type or n-type layers with the metal films can easily be extended to form a ring, as evidenced by the plan view of the invention by Williams (see Figure 7B). *Success* of the implementation of this combination can therefore be *reasonably expected*.

*On claim 2:* said ring-shaped metal film in Williams provided so as to contact with said outermost layer is a gate wiring successively formed with said gate electrode pad 710 (cf. Figure 7B).

*On claim 3:* the one ring-shaped metal film as essentially taught in the above-defined combination of the inventions by Williams et al and Yamamoto is a gate wiring 712 which has gate connecting portions so as to connect to gate electrodes of said transistor cells with partial striding over said protective diode in polysilicon layer 706 (cf. Figure 7A and column 10, line 1), and said gate connecting portions and source connecting portions of said source wiring which are contacted with said most inner layer are alternately formed in plan view (cf. Figure 7B).

*On claim 4:* the p-type and n-type layers in the above-defined combination of the inventions by Williams et al and Yamamoto are made of polysilicon (cf. column 3, lines 58-63 and column 9, line 67 – column 10, line 1).

*On claim 5:* although neither Williams et al nor Yamamoto necessarily teach the further limitation as defined by claim 5, it is understood in the art of semiconductor devices that the subsequent portions of the same conductivity type in the Zener diode, when having roughly the same width and the same impurity concentration, have approximately the same electrostatic breakdown properties so that the electrostatic load be about evenly divided, which is a reasonable choice. However, there is no compelling reason, why the above-mentioned ranges for the ratio of (a) width (around 1) and (b) impurity

concentrations (around 1) is critical to the invention of Applicant, nor does Applicant show such criticality. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

*On claim 6:* the semiconductor device as taught by Williams et al in view of Yamamoto has a diffusion region of P+ conductivity type formed on the closest side to said protective diode of said transistor cells arranged (therein), namely the P+ region abutting region 100A (cf. column 3, line 50 and column 3, lines 35-48) in Figure 1, and said source wiring 112 contacting the innermost layer of said protective diode is contacted (is in direct contact) with said P+ region (see Figure 1). It is observed that said P+ region has no other diffusion region therein: abutting N+ region is a separate diffusion region next to it.

2. ***Claim 9*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al (6,268,242 B1) in view of Yamamoto (JP410144938A) and Throngnumchai et al (4,963,970). Williams et al teach a semiconductor device (cf. title) comprising:

an insulating gate field effect transistor comprising a plurality of transistor cells (separated by a width W; see Figure 1) which are arranged in a semiconductor layer 108 (cf. column 3, lines 39-40) and connected in parallel; and

a protective diode D1 (and D2) (cf. column 3, lines 58-64) connected between a gate and a source of said insulating gate field effect transistor to break down an input of a constant voltage or more applied between said gate and said source (inherent in diode),

wherein said protective diode is formed as a bi-directional diode in which one or more ring-shaped p-type layers and one or more ring-shaped n-type layers 130 (cf. column 3, lines 58-64) are alternately provided on an insulating layer 132 (cf. column 3, line 60) at a peripheral portion of a region of said transistor cells, said protective diode having three or more layers (cf. Figures 1 and 3 in addition to Figure 7B), a source wiring 112 (cf. column 3, line 62) (cf. Figures 7A and 7B) contacts with one layer of said protective diode, and a metal film 134 contacts with another layer of said protective diode (cf. col. 3, l. 58-63), said metal film 134 being successively formed with a gate electrode pad comprising a metal film (cf. col. 3, l. 58-63, Figure 7B) and being ring-shaped (cf. Figure 7B; that the ring is open is another matter, covered by the final sentence of the claim and addressed below in the rejection with regard to it), said one and other layers being positioned at the ends of said protective diode, but arranged in a horizontal direction.

*Williams does not necessarily teach* the metal film 134 to be contacting the full circumferential length of the outermost layer. However, it would have been obvious to improve the invention by Williams to include such ring-shaped contacts in view of Yamamoto, who teaches for the specific purpose of increasing the electrostatic strength

of a Zener diode that said Zener diode and its contact metal be formed so as to *encircle* the cell region (see Abstract, "Problem to be Solved", first sentence).

*Motivation* to include the teaching in this regard by Yamamoto is the consequent improvement of the capability of the Zener diode to protect against electrostatic discharge. The inventions can be *combined* in this regard, because the contact area between the inner – and outermost Zener diode p-type or n-type layers with the metal films can easily be extended to form a ring, as evidenced by the plan view of the invention by Williams (see Figure 7B). *Success* of the implementation of this combination can therefore be *reasonably expected*.

Furthermore, although Williams et al do not teach the arrangement of said protective diode layers to be vertical rather than horizontal, - which implies the limitation "laminated in a height direction". However, it would have been obvious to include said limitation in view of Throngnumchai et al: electrostatic protection of an insulated gate field effect device, particularly as vertical MOSFET device, through a vertically stacked Zener diode, with one innermost or upper p-type layer wired to the source and one outermost or lower n-type layer wired to the gate has long been known in the semiconductor device ESD protection art, as witnessed by Throngnumchai et al, who teach a vertical MOSFET with a Zener diode not flatly formed but instead alternately formed in a height direction, specifically: p-type layer 39 wired to the source S and n-type region 37 wired to the gate G (see Figure 3 , abstract, and column 2, lines 28-56). *Motivation* to include the teaching in this regard by Throngnumchai et al in the invention essentially taught by Yamamoto and Kobayashi et al, or, in the alternative, in the

invention essentially taught by Williams et al and Yamamoto, stems from the obvious savings in lateral real estate by stacking said p- type and n-type layers vertically rather then laterally. The inventions can be easily *combined* by changing the direction of stacking without any consequence to the remainder of the aforementioned inventions. *Success* of the implementation of the combination can therefore be *reasonably expected*.

## ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is: 703-306-0531 BEFORE February 4, 2004; and 571-272-1919 AFTER February 4, 2004. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601 BEFORE February 4, 2004, and on 571-272-1915 AFTER February 4, 2004. The fax phone number for the organization where this application or proceeding is assigned is 703-308-5399.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

JPM
December 29, 2003